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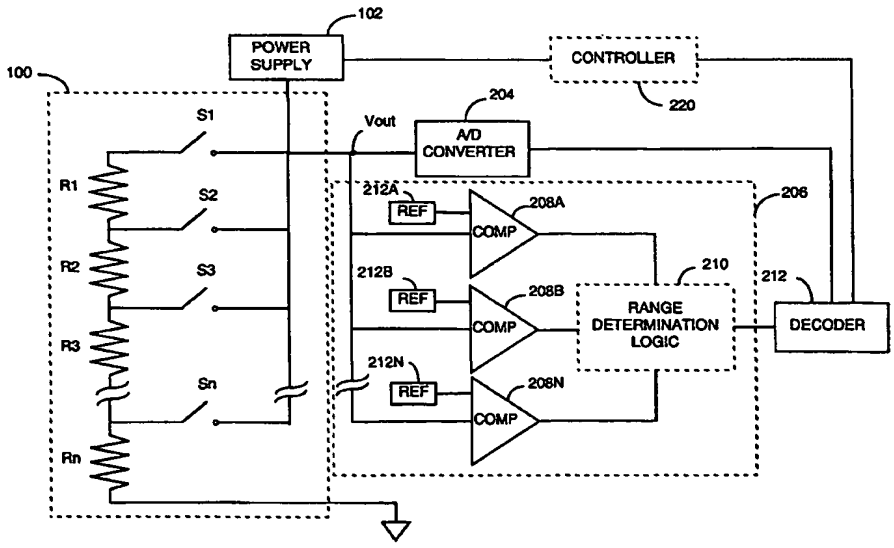

(57) Abstract

A method and circuit for processing switch closures in a passive network (100) having switches (S_1 ... S_n). The passive network (100) generates an output voltage in response to a switch closure. The circuit comprises a comparison circuit (206), coupled to the passive network, for comparing the output voltage to a reference voltage. A decoder (212), coupled to the comparison circuit, decodes the switch closure if the output voltage is within a predetermined range, and does not decode said switch closure if the output voltage is not within the predetermined range. The circuit differentiates between input ranges in a passive network keypad which allows the proper processing of meaningful key presses, while ignoring inadvertent or superfluous key presses, thereby conserving power and processor time.

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DIFFERENTIATING BETWEEN INPUT RANGES IN A PASSIVE KEYPAD

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates to passive keypads. More particularly, the present invention relates to a novel and improved method and circuit for differentiating between various input ranges in a passive keypad.

II. Description of the Related Art

Passive network keypads are well known in the art for use as user input devices. One example of such a passive network keypad is a resistive ladder network. As is known in the art, a resistive ladder network comprises a plurality of resistors connected in series, with each resistor being selectively coupled to a power supply through a respective switch. An exemplary configuration of a resistive ladder network **100** is shown in FIG. 1. Power supply **102** typically includes a voltage or current source, and a pull-up resistor. Resistors R1-Rn are coupled in series. Switches S1-Sn are coupled to bypass or shunt all resistors which are "higher" in the ladder (i.e., closer to the power supply **102** in the series configuration) while coupling the power supply **102** through all remaining resistors which are "lower" in the ladder (i.e., farther away from the power supply **102** in the series configuration). When one of the switches S1-Sn is closed, a corresponding voltage, Vout, appears across the output terminals of the resistive ladder **100**. The magnitude of the output voltage Vout depends on which switch S1-Sn was closed.

For example, if switch S3 is closed, current from power supply **102** flows through S3, bypassing resistors R1 and R2. The current flows through resistors R3 through Rn. Thus, by Ohm's law, the output voltage Vout for the closure of any switch, Sx, will equal:

$$\text{Vout} = i^* \sum_{j=x}^{n} Rj \qquad (1)$$

where i is equal to the current generated by power supply **102**, n is the total number of switches in the resistive ladder, and Rj is the jth resistor in the resistive ladder.

Since it is easy to calculate the expected output voltage for each switch closure, and thereby determine which switch was pressed, resistive ladder networks are convenient ways to encode a passive network keypad. And since passive network keypads require no active components to function, they are desirable for use in portable electronic equipment because they consume no power when in their static state. Thus, passive network keypads are particularly suitable for use as input devices in wireless communication devices such as cellular or PCS-band wireless telephones.

However, one drawback to using a passive network keypad in a wireless communication device is that it generates only an analog voltage level as an output. As such, the analog voltage level must be decoded in order to determine which key was pressed. Decoding which key was pressed requires the operation of a processor which consumes current, which thereby drains the battery in the wireless communication device. Furthermore, decoding which key was pressed also requires processor time, which takes time away from other functions that the processor may be performing at the time the key was pressed. If the keypress was inadvertent or superfluous, then the current and time spent by the processor to decode which key was pressed is wasted.

An additional drawback of a typical passive network keypad in a wireless communication device is that the processor typically must poll an analog-to-digital converter (ADC) at the output of the keypad at some predefined interval to detect key presses. To the extent that the processor is polling the keypad ADC when no keys have been pressed, this also uses processor time and current unnecessarily.

What is needed is a method and circuit for differentiating between input ranges in a passive network keypad which allows the proper processing of meaningful keypresses, while ignoring inadvertent or superfluous keypresses, and while avoiding excessive polling of the keypad, thereby conserving power and processor time.

SUMMARY OF THE INVENTION

The present invention is a novel and improved method and circuit for processing switch closures in a passive network having switches. The passive network generates an output voltage in response to a switch closure. The circuit comprises a comparison circuit, coupled to the passive network, for comparing the output voltage to a reference voltage. A decoder, coupled to the comparison circuit, decodes the switch closure if the output voltage is

within a predetermined range, and does not decode said switch closure if the output voltage is not within the predetermined range.

In the preferred embodiment, the comparison circuit comprises at least one comparator, each comparator having a first input coupled to the passive network. A respective reference voltage generator is coupled to a second input of each one of the comparators. Each of the reference voltage generators generates a respective reference voltage which define the predetermined range.

In one embodiment, the comparison circuit further comprises a range determination logic circuit coupled to each of the comparator outputs. The range determination logic distinguishes between different ranges of the output voltages generated by the passive network.

Also in the preferred embodiment, the comparison circuit comprises a first comparator for generating a comparison signal only if a first predetermined subset of the switches is closed; and a second comparator for generating a comparison signal only if a second predetermined subset of switches is closed. In this embodiment, the comparison circuit generates an interrupt signal to the decoder only if the output voltage is within the predetermined range, which corresponds to a predetermined subset of switches. The predetermined subset of switches may include a power switch. In such a case, the comparison circuit generates an interrupt signal to the decoder only if the power switch is closed.

In another embodiment, the circuit further comprises a controller, coupled to the decoder, for altering an input voltage of the passive network in response to the decoder decoding said switch closure. By altering the input voltage of the passive network, the output voltage range is likewise altered. As a result the subset of switches which generate an interrupt is altered for a given comparison reference voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

FIG. 1 is a circuit-level diagram of a resistive ladder network;

FIG. 2 is a functional block diagram of the circuit of the present invention;

FIG. 3 is a circuit-level diagram of a preferred embodiment of the reference voltage generators and comparators of FIG. 2; and

FIG. 4 is a flow diagram of the method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is applicable to any portable or fixed electronic equipment which uses a passive network to encode a user input, such as a keypad. Thus, the present invention is particularly applicable to portable electronic devices such as wireless communication devices in which it is desirable to conserve battery power and processor compute time. As defined herein, "key press" means any activation of the user input, for example the pressing of a mechanical keyswitch on a standard telephone keypad.

Turning now to FIG. 2, a functional block diagram of the circuit of the present invention is illustrated. Resistive ladder network **100** and power supply **102** are identical to those described with reference to FIG. 1. Thus, the magnitude of the voltage Vout is dependent upon which switch S1-Sn was closed.

An analog to digital converter (A/D) **204** converts the analog voltage Vout to a digital key press signal representative of which switch S1-Sn was closed, for example by the user pressing an associated keyswitch on a keypad (not shown). As is known in the art, A/D converter **204** samples Vout at a predetermined rate to generate the digital keypress signal. A/D converter **204** may be any off-the-shelf A/D converter of any suitable bit width as is known in the art. For example, A/D converter may generate a 5-bit wide digital keypress signal, thereby being able to distinguish among 2^5 different levels of Vout. Such a configuration would be able to support 32 different switches S1-S32.

A/D converter **204** passes the digital keypress signal to decoder **212** for determination of which switch was closed. Decoder **212** determines, from the digital keypress signal generated by A/D converter **204**, which switch S1-Sn was closed. For example, decoder **212** may compare the digital keypress signal to a correspondence table of stored values. Each value in the correspondence table may correspond to a particular keypress. Alternately, decoder **212** may perform a mathematical operation on the digital keypress signal to determine which switch S1-Sn was closed. Decoder **212** may comprise any general purpose microprocessor and associated memory programmed to perform the decoding operation described herein.

As discussed above in the Background of the Invention, decoding which key was pressed requires the operation of a decoder **212** which consumes current, which thereby drains the battery in the wireless communication device. Furthermore, decoding which key was pressed also requires processor time, which takes time away from other functions that the processor to which decoder **212** may belong may be performing at the time the key was pressed. If the key press was inadvertent or superfluous, then the current and time spent by the processor to decode which key was pressed is wasted.

This is particularly true if the wireless communication device using the resistive ladder network **100** operates in a "sleep" mode, whereby it powers down the majority of its hardware components, including decoder **212** and A/D converter **204** when they are not required. Using this sleep mode conserves battery power, leading to longer operating and standby times.

In order to avoid consuming decoder **212** processing cycles, or waking up decoder **212** when it is powered down, the present invention utilizes a comparison circuit **206** to gate or screen interrupts to decoder **212**.

An exemplary first embodiment of comparison circuit **206** is illustrated in FIG. 2. In this embodiment, comparison circuit **206** preferably comprises at least one comparator **208A-208N**, and a corresponding at least one reference voltage generator **212A-212N**. One input of the at least one comparator **208A-208N** is coupled to the Vout terminal of resistive ladder network **100**. A second input of the at least one comparator **208A-208N** is coupled to the output of the corresponding at least one reference voltage generator **212A-212N**. In the preferred embodiment, each reference voltage generator **212A-212N** generates a different reference voltage level for its corresponding comparator **208A-208N**.

In operation, each comparator **208A-208N** senses the voltage level Vout and compares it with the reference voltage generated by its corresponding reference voltage generator **212A-212N**. Each comparator **208A-208N** then outputs a comparison signal indicative of the result of the comparison. For example, in the preferred embodiment if the voltage Vout is less than the threshold reference voltage, then the comparator **208A-208N** outputs a logic level "high". If, on the other hand, the voltage Vout is greater than the threshold reference voltage, then the comparator **208A-208N** outputs a logic level "low". In other words, in the preferred embodiment, the comparators **208A-208N** are configured as "less than" type

comparators. In alternate embodiments, comparators **208A-208N** may be configured as "greater than" type comparators.

Comparators **208A-208N** is preferably any suitable off-the-shelf op-amp comparator as is known in the art. However, there are many other means for comparing two signals that are known in the art. For example, a transistor gate, a zener diode, or other device as is known in the art may be used in place of comparators **208A-208N**, and indeed the whole of comparison circuit **206**.

Reference voltage generators **212A-212N** are preferably resistive voltage divider circuits and an associated power supply. For example, power supply **102** may be divided down by resistive voltage dividers internal to reference voltage generators **212A-212N** to generate the respective threshold reference voltages. An exemplary implementation of comparators **208A-208B** and reference voltage generators **212A-212B** is illustrated in FIG. 3.

In FIG. 3, power supply **102** is divided down by resistors Ra and Rb to provide the threshold reference voltage for comparator **208A**. Likewise, resistors Rc and Rd generate the threshold reference voltage for comparator **208B**. The choice of the value of resistors Ra-Rd is dependent on the threshold voltage level that is desired for Vout to meet before the comparators **208A** and **208B** are triggered.

In the preferred embodiment, the range for Vout is from about .01 volts to 1.5 volts. In other words, the values of resistors R1-Rn (FIG 2) are chosen such that when switch Sn (FIG. 2) is closed, the voltage level of Vout is about .01 volts, and when switch S1 is closed, the voltage level of Vout is about 1.5 volts. Thus, if it is desired that only switch Sn trigger comparator **208N**, then the values of Rc and Rd are chosen such that the threshold reference voltage for comparator **208N** is greater than .01 volts. For the exemplary power supply voltage of 3.3 volts, an exemplary choice for Rc is 1 Megohm, and Rd is 30.9 Kilohms. Furthermore, if it is desired that any switch S1-Sn trigger comparator **208A**, then for the exemplary power supply voltage of 3.3 volts, an exemplary choice for Ra is 511 Kilohms, and Rb is 453 Kilohms.

Referring again to FIG. 2, the outputs of comparators **208A-208N** may be coupled to optional range determination logic **210**. Range determination logic **210** functions to distinguish which range or subset of switches S1-Sn has been closed. For example, if comparator **208A** is configured to trigger as described above for any switch S1-Sn, and comparator **208B** is configured to trigger as described above only for switch Sn, then simple combinatorial logic (i.e., an AND gate with one inverted input) will be able to determine

whether one of the switches in the range S1-Sn-1 was closed (i.e., Vout < 1.5 volts, and not Vout < .1 volts). It will be clear to one of ordinary skill in the art that by configuring the threshold voltages, higher-than or lower-than comparisons, and range determination logic **210** to various combinations, it is possible to distinguish among any range of switch closures S1-Sn as desired.

The physical implementation of comparison circuit **206** does not limit the present invention. The number of comparators **208A-208N**, the type of comparison utilized, and the range determination logic **210** may be accomplished in many different ways without departing from the present invention.

In summary, comparison circuit **206** functions to allow only certain predetermined switch closures, or combination of switch closures, to generate an interrupt signal to decoder **212**. For example, if the present invention is implemented in a wireless communication device which utilizes sleep modes to conserve battery power, the comparison circuit **206** may be configured to generate an interrupt to decoder **212** only when switch Sn is closed, where switch Sn corresponds to a "Power On" key. In such a case, decoder **212** would wake up to read A/D converter **204** only when the "Power On" key was pressed. In this way, the wireless communication device utilizing the present invention would be able to power down decoder **212** and A/D converter **204** completely and still be able to wake up and read the keypad input when required. Additionally, the present invention allows a partially or fully interrupt-driven method of operation, whereby the decoder **212** is not required to actively poll A/D converter **204**, but rather may be configured only to poll A/D converter **204** when an interrupt is generated by comparison circuit **206**.

In other words, a specific application of the circuit of FIG. 2 is to prevent all other keys except the "Power On" key from waking up the decoder **212** when it is powered off. This will be useful, for example, if the wireless communication device is carried in a purse or briefcase where it may contact foreign objects which inadvertently activate the keypad. In such a case, it is desirable to ignore all key presses except for the "Power On" key to avoid spending time and power evaluating superfluous key presses.

Another application of the circuit of FIG. 2 is to prevent all but a specific range of keys from interrupting the processor of which decoder **212** may be a part. This will be useful, for example, when the user is scrolling through menus in which only a subset of keys represent valid inputs. In

such a case, it would also be desirable to ignore all invalid key presses to avoid spending time and power evaluating superfluous key presses.

In another embodiment, decoder **212** may, upon detecting a predetermined switch closure or combination of switch closures, notify controller **220** that the predetermined switch closure was detected and decoded. In response to this closure, controller **220** directs power supply **102** to alter the input voltage to resistive ladder network **100**, for example, by turning on or off a switchable voltage or current source, or varying a variable voltage or current source. By altering the input voltage to resistive ladder network **100**, the output voltage Vout will be shifted by a corresponding amount for each switch closure. In other words, if the input voltage to resistive ladder network **100** is increased by 1 volt, a corresponding 1 volt shift in Vout for each switch closure will be observed.

If the threshold reference voltages generated by reference voltage generators **212A-212N** remain constant when the input voltage to resistive ladder network **100** is altered, the range of switches S1-Sn which trigger each comparator **208A-208N** will likewise be altered. Thus, continuing the above example where comparator **208N** was only triggered by the closure of switch Sn at, if the input voltage to resistive ladder network **100** is lowered sufficiently, then comparator **208N** may also be triggered by the closure of switch Sn-1. Alternately, it is clear that one can also keep the input voltage to resistive ladder network **100** constant, and instead alter the threshold reference voltages generated by reference voltage generators **212A-212N** in order to "shift" the range of switches S1-Sn which trigger each comparator **208A-208N**.

It can easily be seen that by altering the input voltage to resistive ladder network **100**, the corresponding shift in the range of Vout may be used to allow a different range of key presses to generate interrupts to decoder **212**. A useful application of this facet of the present invention is to assign the "Power On" functionality to switch Sn, and configuring comparison circuit **206** to generate an interrupt for decoder **212** only when a voltage as small as the one generated by the closure of switch Sn is present at Vout. Then, upon detecting and decoding the closure of switch Sn in decoder **212**, controller **220** directs power supply **102** to lower the input voltage to resistive ladder network **100** sufficiently that the closure of any switch S1-Sn generates an interrupt to decoder **212**. In this manner, only pressing the "Power On" key will wake up decoder **212**, but thereafter and key press will trigger an interrupt to cause decoder **212** to read the output of A/D converter **204**.

Controller **220** may be any microprocessor or microcontroller as is known in the art, and furthermore may be advantageously combined with decoder **212** in the same programmable general purpose microprocessor. Various other configurations of the circuit of FIG. 2 will be apparent to one of ordinary skill in the art. For example, any of the elements of FIG. 2 may be configured to operate based on current levels rather than voltage levels.

In still another embodiment, A/D converter **204** may be removed completely, and comparison circuit **206** may be configured to generate an interrupt for each key pressed. For only a few switches, this may be less expensive. Also, even on a complex keypad, the comparison circuit **206** may be read in fewer processing cycles. This alternate embodiment may be used to encode a keyboard over a long wiring distance, and convert it back into a matrix using comparators and logic.

Turning now to FIG. 4, a flowchart of the method of the present invention is shown. The process begins at block **402** where a voltage is generated in a passive network, for example the resistive ladder **100** of FIG. 2, in response to a key press. At block **404**, the voltage is compared to a reference voltage, for example in comparison circuit **206** of FIG. 2. At decision **408**, it is determined whether the generated voltage is within a predetermined range. If it is not, the key press which initiated the voltage is ignored (i.e., no processor or decoder action is taken on it).

If on the other hand, it is determined at decision **408** that the generated voltage is within a predetermined range, then the keypress which generated the voltage is decoded, for example in decoder **212** of FIG. 2. Optionally, the flow continues to block **412** where the input voltage to the passive network is altered, for example as described above with respect to controller **220**. In either case, the flow returns to block **402** to generate a voltage in response to the next key press.

As described above, the present invention is a method and circuit for differentiating between input ranges in a passive network keypad which allows the proper processing of meaningful keypresses, while ignoring inadvertent or superfluous keypresses, thereby conserving power and processor time.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the

embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WE CLAIM:

CLAIMS

1. A circuit for processing switch closures in a passive network having switches, said passive network generating a voltage in response to a switch closure, the circuit comprising:

a comparison circuit, coupled to said passive network, for comparing said voltage to a reference voltage; and

a decoder, coupled to said comparison circuit, for decoding said switch closure if said voltage is within a predetermined range, wherein said decoder does not decode said switch closure if said voltage is not within said predetermined range.

2. The circuit of claim 1 wherein said comparison circuit comprises:

at least one comparator, each comparator having a first input coupled to said passive network and having a second input and an output for generating a comparison signal; and

at least one reference voltage generator, each reference voltage generator coupled to said second input of a respective one of said comparators, each of said reference voltage generators for generating a respective reference voltage;

wherein said predetermined range is defined by said reference voltages.

3. The circuit of claim 2 wherein said comparison circuit further comprises a range determination logic circuit coupled to each of said comparator outputs, said range determination logic for distinguishing between different ranges of said voltages generated by said passive network.

4. The circuit of claim 2 wherein said comparison circuit comprises:

a first comparator for generating said comparison signal only if a first predetermined subset of said switches is closed; and

a second comparator for generating said comparison signal only if a second predetermined subset of switches is closed.

5. The circuit of claim 1 wherein said comparison circuit generates an interrupt signal to said decoder only if said voltage is within said predetermined range.

6. The circuit of claim 5 wherein said predetermined range corresponds to a predetermined subset of said switches.

7. The circuit of claim 6 wherein said predetermined subset of switches includes a power switch, and wherein said comparison circuit generates an interrupt signal to said decoder only if said power switch is closed.

8. The circuit of claim 1 further comprising a controller, coupled to said decoder, for altering an input voltage of said passive network in response to said decoder decoding said switch closure.

9. A method for processing switch closures in a passive network having switches, said passive network generating a voltage in response to a switch closure, the method comprising the steps of:

comparing said voltage to a reference voltage;

decoding said switch closure if said voltage is within a predetermined range; and

ignoring said switch closure if said voltage is not within said predetermined range.

10. The method of claim 9 wherein said predetermined range is defined by said reference voltage.

11. The method of claim 10 further comprising the step of distinguishing between different ranges of said voltages generated by said passive network.

12. The method of claim 9 further comprising the step of generating an interrupt signal only if said voltage is within said predetermined range.

13. The method of claim 12 wherein said predetermined range corresponds to a predetermined subset of said switches.

14. The method of claim 13 wherein said predetermined subset of switches includes a power switch, and wherein said step of generating an interrupt signal only if said voltage is within said predetermined range

4 comprises generating said interrupt signal only if said power switch is closed.

15. The method of claim 9 further comprising the step of altering 2 an input voltage of said passive network in response to said decoder decoding said switch closure.

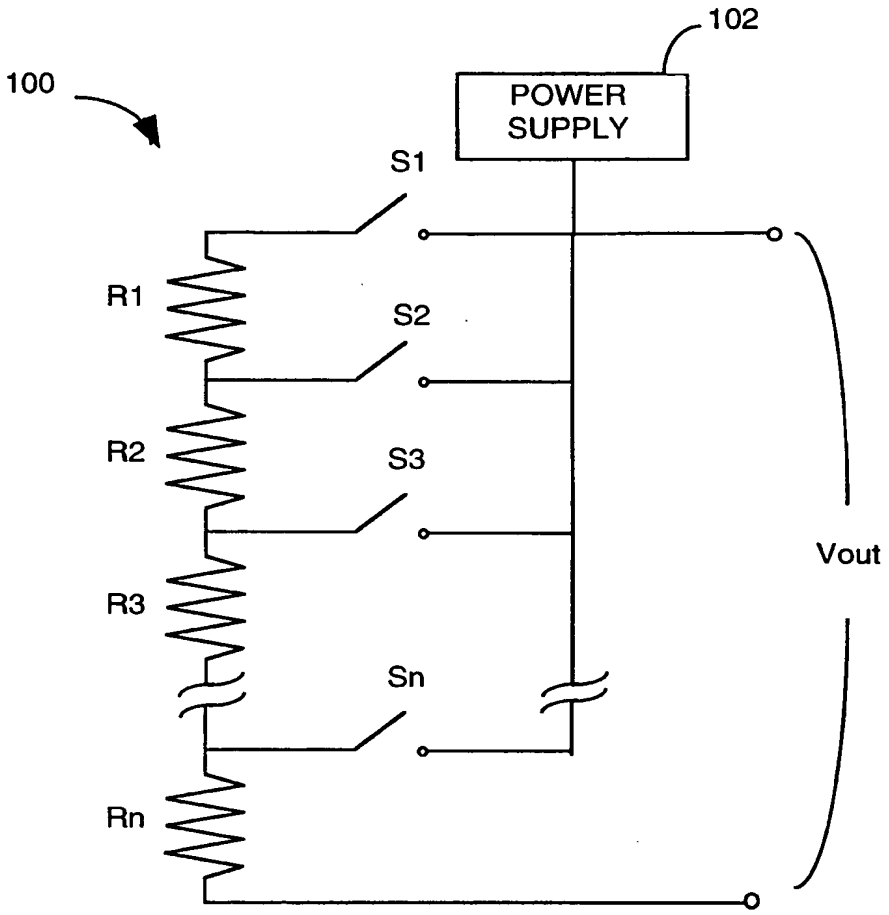

FIG. 1

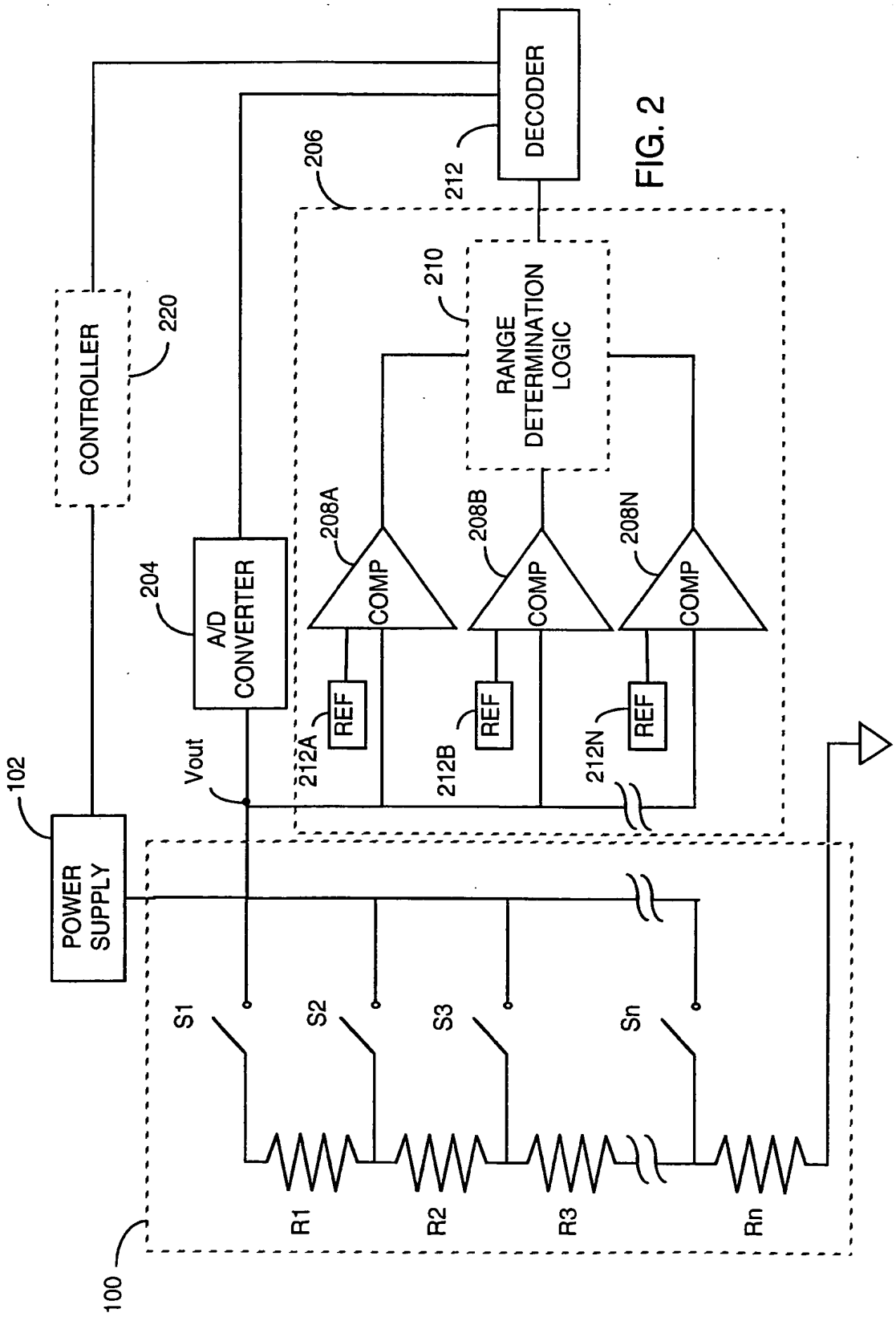
DECODER
206
212
210
RANGE DETERMINATION LOGIC
CONTROLLER
220
208A
208B
208N
COMP
COMP
COMP
204
A/D CONVERTER
REF
REF
REF
212A
212B
212N
Vout
102
POWER SUPPLY
S1
S2
S3
Sn
R1
R2
R3
Rn
100

FIG. 2

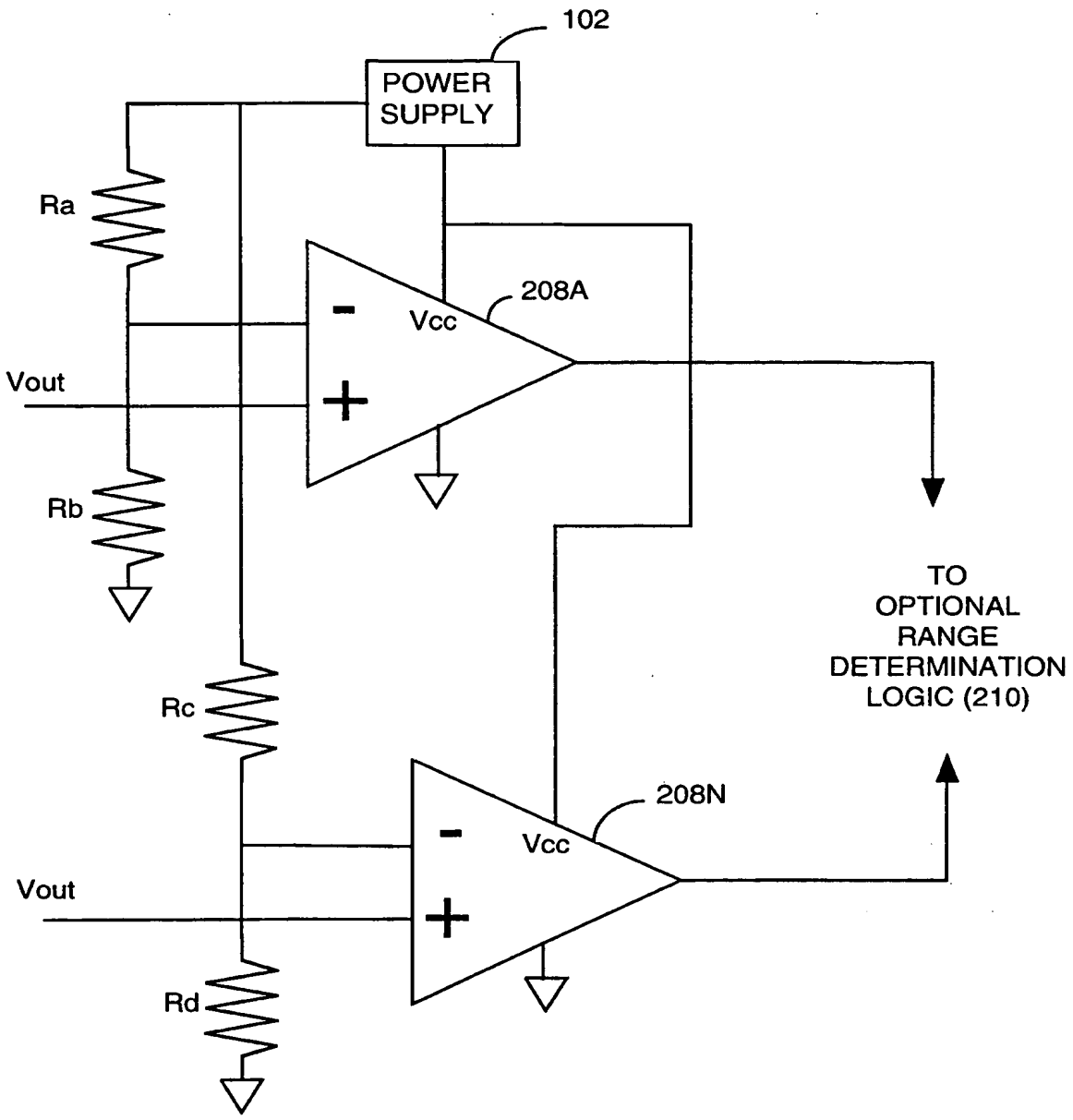
102
POWER SUPPLY
Ra
208A
Vcc
Vout
Rb
TO OPTIONAL RANGE DETERMINATION LOGIC (210)
Rc
208N
Vcc
Vout
Rd

FIG. 3

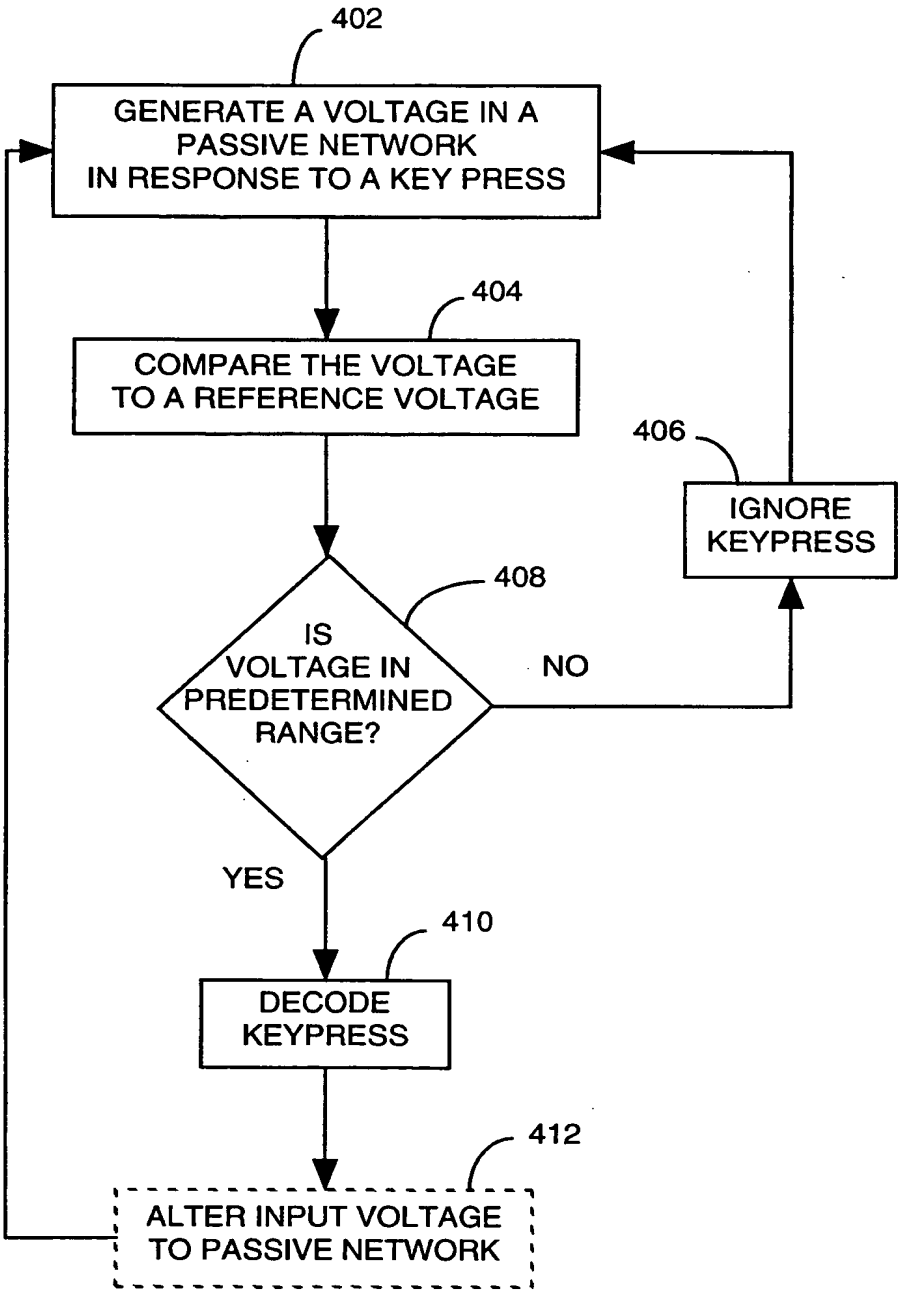
402
GENERATE A VOLTAGE IN A PASSIVE NETWORK IN RESPONSE TO A KEY PRESS
404
COMPARE THE VOLTAGE TO A REFERENCE VOLTAGE
406
IGNORE KEYPRESS
408
IS VOLTAGE IN PREDETERMINED RANGE?
NO
YES
410
DECODE KEYPRESS
412
ALTER INPUT VOLTAGE TO PASSIVE NETWORK

FIG. 4

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/US 99/11412

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03M11/24 H03M1/00 H03M1/18 //H03M1/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 43 28 663 C (GRUNDIG EMV) 9 June 1994 (1994-06-09) column 3, line 14 -column 4, line 40; figures 1,2	1-6,9, 10,12,13
A	US 5 343 200 A (MATSUI HISAYOSHI) 30 August 1994 (1994-08-30) figure 5	1,9

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 September 1999	30/09/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (-31-70) 340-2040, Tx. 31 651 epo nl, Fax: (-31-70) 340-3016	Beindorff, W

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Interr ·nal Application No
PCT/US 99/11412

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 4328663 C	09-06-1994	EP 0641086 A	01-03-1995
US 5343200 A	30-08-1994	JP 4267629 A	24-09-1992
		JP 4111536 A	13-04-1992